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| 0.2 | 11-Dec-2020 | Notice that was not proper tracking of this document. I will start tracking now | Juan F. Osorio |
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| 0.13 | 19-Nov-2021 | Create initialization procedures | Juan F. Osorio |
| 0.14 | 09-Dec-2021 | Including mode description for the IF-BIST modes | Juan F. Osorio |
| 0.15 | 21-Dec-2021 | Include the different modes | Juan F. Osorio |

Revision history

Contents

[1. Document purpose 4](#_Toc90993698)

[2. Generate architecture 4](#_Toc90993699)

[3. On the relation of the filter and the timing engine 5](#_Toc90993700)

[3.1 Available signals from the Timing Engine 6](#_Toc90993701)

[4. IF Saturation detector 6](#_Toc90993702)

[4.1 . Digital functionality 7](#_Toc90993703)

[4.2 . Saturation DAC range and step 7](#_Toc90993704)

[4.3 . Functional safety 9](#_Toc90993705)

[5. Filter Dynamic Control During Chirp Resets 10](#_Toc90993706)

[6. LO Level Detector 13](#_Toc90993707)

[6.1.1 Calibration of the LO level detector 13](#_Toc90993708)

[6.1.2 Functional safety test 13](#_Toc90993709)

[7. Functional Safety Rx Subsystem 13](#_Toc90993710)

[7.1 Ball brake detector 13](#_Toc90993711)

[8. IF-BIST 14](#_Toc90993712)

[8.1 IF BIST Modes and sequence 14](#_Toc90993713)

[8.2 IF-BIST and Central Baseband BIST power-on / power -off sequence 16](#_Toc90993714)

[Assumptions: 16](#_Toc90993715)

[Power-on Sequence 16](#_Toc90993716)

[Power-off sequence 16](#_Toc90993717)

[9. RF BIST 16](#_Toc90993718)

[10. Initialization and programming sequences 18](#_Toc90993719)

[10.1 . Top level sequences 18](#_Toc90993720)

[10.2 BIST 18](#_Toc90993721)

[11. ATB 18](#_Toc90993722)

[12. References 18](#_Toc90993723)

[13. Test Vehicle circuits descriptions 19](#_Toc90993724)

[13.1 IF Saturation detector (TV) 19](#_Toc90993725)

[13.1.1 Digital functionality 19](#_Toc90993726)

[13.1.2 Saturation DAC range and step 19](#_Toc90993727)

[13.2 . LO Level Detector 20](#_Toc90993728)

[13.2.1 Calibration of the LO level detector 21](#_Toc90993729)

[13.3 Extra description in the saturation detector (Vinoth) 21](#_Toc90993730)

[14. Distribution 22](#_Toc90993731)

# Document purpose

This document describes the functionality and implementation of the functions that are specific for the Rx digital subsystem.

The digital subsystem is in charge of the control of the Rx. Every receiver has a digital interface as described in [REF] (TODO: add reference to the general document). Most of the functionality is similar for the different IP except for some functionality that in the case of the Rx is described in this document

# Generate architecture

**Figure 1** Shows the full diagram of the circuit is a functional diagram of the Rx, the complementary **Figure 2** shows the functionality of the Filter and the IF-BIST and its connection with the ADC.

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| Diagram  Description automatically generated |
| **Figure 1. Figure of the complete Rx. The dotted line shows the CMOS part of the chip. The input balun is implemented using the laminate** |

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| Diagram, schematic  Description automatically generated |
| **Figure 2. Filter architecture including IFBIST and connection with the ADC** |

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| A picture containing diagram  Description automatically generated |
| **Figure 3. LNA detail figure of the LNA** |

# On the relation of the filter and the timing engine

Beside defining several static control signals the digital subsystem has other functions. That is processing the functional safety flags coming from the analog circuitry and also providing dedicated dynamic functionality synchronized using the timing engine.

The main dynamic functions associated with the timing engine in the RX are:

* The power-on and power down of the analog circuits. Described in section: TODO
* A part of the functionality of the saturation detector is implemented in the digital circuit. Described in section 3.2
* The dynamic control of the filter during resets. Section 3.3

## Available signals from the Timing Engine

The timing engine provide signals signal to synchronize the different radar functions, those signals are defined in a 40MHz timestamp. The signals available from the timing engine in the Rx digital subsystem are shown here for completeness. The signals from the timing engine are required for the dynamical functionality of the Rx analog.

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|  |
| **Figure 3: The signals available from the timing engine and their relationship with the timing of the chirp. Except for: Chirp\_Start, Data\_acquision\_active, Safety\_monitor\_active are not present in the other signals are present in the Rx Digital Subsystem.** |

# IF Saturation detector

The saturation detector is used in the filter to detect that the level of the signals overpass certain predefined level. There is a complete documentation of this module that can be found in collabned [1]. This section here would focus only in the requirements for the digital circuit. The next figure shows the diagram of the saturation detector.

## . Digital functionality

The circuit is made of a digital circuit and analog circuit. The Saturation detector uses a differential latch together with a logarithmic-DAC to achieve a large dynamic range programmability. The saturation detector is reset every 25ns using a pulse that is always small than 2ns. When the signal at the output of the VGA is higher than the voltage output of the log-DAC the flag is stored in a SR and is capture by the digital circuit in the falling edge.

The digital circuit would measure the number of events happening in the analog signal when the signal safety\_monitor\_active\_te is enabled. After an extended period, typically a radar frame, the number of errors are counted and are compared with a programed word of 22bits.

In order to avoid metastability problems the value of the SR latch is sampled in the digital side using a negative-edged flip-flop.

Even where there are 4 saturation detector per Rx there are only 2 digital circuits as the analog outputs of the circuits I/Q are combined in a single output error\_status\_sat\_vga[x]\_err per stage. Stage 1 or 2.

## . Saturation DAC range and step

The saturation detector uses la logarithm-DAC to define the value that make triggers it. The DAC is implemented as a logarithm resistor divider which uses as a reference the same LDO that the filter. The saturation detector threshold voltages are defined as:

The dependence of the *vsat* with the voltage of the ldo, *vldo*, is intended as the linearity of the filter depends primarily on the ratio of the output peak signal and the vldo.

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| **Diagram, schematic  Description automatically generated** |
| **Figure 4. Saturation detector. Analog section of the circuit.** |

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| **Figure 5. Saturation detector. Digital section of the circuit. In bold: signals stored in registers, in italic: signals coming from the timing engine.** |

## . Functional safety

The current sensor can be tested by forcing the signal test\_force\_error\_sat\_vga[x]\_force. There are two of this signal corresponding with the sensor for vga1, [x]=1 and vga2, [x]=2. During this test the rx\_force\_error signal is enabled such as one single count coming from the analog circuit triggers the digital comparator.

There are two comparators per saturation detector, due to the differential nature of the signal. One of them for the differential signal going above the threshold: vdiff > vth and another for the vdiff signal going below the threshold that is vdiff < -vth.

In total there are then 8 comparators in the analog circuit and 2 in the digital.

|  |  |  |  |
| --- | --- | --- | --- |
| Stage | I/Q | Vdiff | Test |
| Vga1 | I | >vth | test\_force\_error\_sat\_vga1\_force=1  sat\_det\_comp\_pos\_en\_meas = 1  sat\_det\_comp\_neg\_en\_meas = 0  sat\_det\_dig\_st1\_sel\_error<1:0> = 1 |
| Vga2 | I | >vth | test\_force\_error\_sat\_vga2\_force=1  sat\_det\_comp\_pos\_en\_meas = 1  sat\_det\_comp\_neg\_en\_meas = 0  sat\_det\_dig\_st2\_sel\_error<1:0> = 1 |
| Vga1 | Q | >vth | test\_force\_error\_sat\_vga1\_force=1  sat\_det\_comp\_pos\_en\_meas = 1  sat\_det\_comp\_neg\_en\_meas = 0  sat\_det\_dig\_st1\_sel\_error<1:0> = 2 |
| Vga2 | Q | >vth | test\_force\_error\_sat\_vga2\_force=1  sat\_det\_comp\_pos\_en\_meas = 1  sat\_det\_comp\_neg\_en\_meas = 0  sat\_det\_dig\_st2\_sel\_error<1:0> = 2 |
| Vga1 | I | <-vth | test\_force\_error\_sat\_vga1\_force=1  sat\_det\_comp\_pos\_en\_meas = 0  sat\_det\_comp\_neg\_en\_meas = 1  sat\_det\_dig\_st1\_sel\_error<1:0> = 1 |
| Vga2 | I | <-vth | test\_force\_error\_sat\_vga2\_force=1  sat\_det\_comp\_pos\_en\_meas = 0  sat\_det\_comp\_neg\_en\_meas = 1  sat\_det\_dig\_st2\_sel\_error<1:0> = 1 |
| Vga1 | Q | <-vth | test\_force\_error\_sat\_vga1\_force=1  sat\_det\_comp\_pos\_en\_meas = 0  sat\_det\_comp\_neg\_en\_meas = 1  sat\_det\_dig\_st1\_sel\_error<1:0> = 2 |
| Vga2 | Q | <-vth | test\_force\_error\_sat\_vga2\_force=1  sat\_det\_comp\_pos\_en\_meas = 0  sat\_det\_comp\_neg\_en\_meas = 1  sat\_det\_dig\_st2\_sel\_error<1:0> = 2 |

Table 1 Functional safety test for every comparator in the analog circuit

# Filter Dynamic Control During Chirp Resets

During chirp resting the signal in the filter changes so rapidly that it may create a large step in the high pass filter. As this filter uses a big capacitor this might get charged to a DC value and would require time to settle properly before acquisition. Two actions are taken to avoid that. First the filter is momentary settles to its *high bandwidth state* and the switch between the two different circuits is open.

This depends on the information coming from the timing engine, specifically on the signal *rx\_hp\_reset\_via\_tim\_eng* that as indicated by its name comes from the timing engine. (TODO) add diagram of Filter dynamic control

**Figure 6** shows the signals involved in this control. This is the signals settling the filter transfer function plus the switch between the two VGA. The signals for the four capacitors banks, if\_st1\_cin, if\_st1\_cf, if\_st2\_cin, if\_st2\_cf are subdivided in different separate groups as shown in below the plot. For the purpose of the Filter Dynamic Control During Chirp resets (FDC), this would be treated as a single bus.

|  |
| --- |
| Diagram  Description automatically generated |
| **Figure 6: The signals available from the timing engine and their relationship with the timing of the chirp. Except for: Chirp\_Start, Data\_acquision\_active, Safety\_monitor\_active are not present in the other signals are present in the Rx Digital Subsystem.**  **This also shows the correspondence with the register map as defined in** [2] |

All the signals involved in this operation are part of the profiles except for rx\_active\_comb\_n, which comes directly from the register value.

After the multiplexer selects the signal from the right profile, this is multiplexed with the signals terminating starting to hpf\_rst. Those signals do not need to be used in the profile. There are a total of eight of this structures as some of them repeat in the stage 1 (st1) and the stage 2(st2) of the filter.

The signal rf needs to be decoded from binary to 1-hot bit. The output is 35 bits so this would be stored in a 6 bits word in the registers with only 35 values being valid (the less significant bits).

|  |  |
| --- | --- |
| Binary code | if\_st1\_rf<34:0> |
| 0 | 000…001 |
| 1 | 000…010 |
| … | … |
| 33 | 010…000 |
| 34 | 100…000 |

Table 2 Encoding for the rf signal

Finally, due to debugging purposes, the change of this fast reset can be overwritten by the signal if\_hp\_rst\_overwrite, in which cases the filter will have the static values coming from the if\_hp\_rst portion of the register.

|  |
| --- |
| Diagram  Description automatically generated |
| **Figure 7: Glue logic required the FDC and extra decoder is require in the digital for the signals if\_st1\_rf and if\_st2\_rf. In Bold signals coming from the register and in italic signals coming from the timing engine.** |

# LO Level Detector

In order to ensure the mixer it is properly switch it is necessary to verify the level of the LO signal. For that a level detector circuit is used. This circuits is shown in **Figure 12**. The circuit compares the DC output level of the output of the DAC with the rectified version of the 78GHz signal.

### Calibration of the LO level detector

Before every radar cycle the level lo needs to be set such as the reliability of the mixer transistor is maintain. For that the LO level detector is programmed to detect a high level and the Lox2 buffer (TODO: add more reference) is swept until the flag toggles. The LO signal is set one step less.

During acquisition the LO level detector is programmed to detect the minimum acceptable signal in the LO.

|  |
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| Diagram, schematic  Description automatically generated |
| **Figure 8: LO Level Detector** |

### Functional safety test

The signal test\_force-error\_mixer\_i\_lo\_force can be used to increase the voltage of the DAC causing the comparator to report and error checking the comparator. TODO: Define if the lo signal is present during the test.

# Functional Safety Rx Subsystem

## Ball brake detector

The ball brake detector is used to detect if there is a DC open circuit in one of the package connections of a ball missing. The below diagram shows a functional diagram of the BBD.

in order to operate the BBD requires that there is a DC path between the mm-wave signal and the ground at the PCB level. If this circuit is open and the BBD is operational there would be large voltage difference between the two terminal voltages.

A switch is provided to ground one of the input of the detector and create a false error and that can be used to verify that the comparator is working properly.

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| A picture containing diagram  Description automatically generated |
| **Figure 9: Ball break detector functional diagram shown the return path of the current when the system is functional** |

# IF-BIST

## IF BIST Modes

The BIST can be configured in several ways. There are described in the figures below. Compared with previous documents this includes an extra mode, Mode 5, to be used during validation with an external equipment.

|  |
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|  |
| Figure 13 Mode 0. Default mode, used during normal operation. Mode 1, used to measure the filter transfer function |

|  |
| --- |
|  |
| Figure 13 Mode 2 Mode 3 Default mode used during normal operation |

|  |
| --- |
|  |
| Figure 12. Mode 4 and Mode 5 |

Routines associated with this modes can be found in:

|  |  |
| --- | --- |
| Registers used | Comments |
| bist/idaSTRX\_RX1\_IFBIST\_MODE1\_enable.bf | Mode1 programing for RX1 |
| bist/idaSTRX\_RX1\_IFBIST\_MODE2\_enable.bf | Mode2 programing for RX1 |
| bist/idaSTRX\_RX1\_IFBIST\_MODE3\_enable.bf | Mode3 programing for RX1 |
| bist/idaSTRX\_RX1\_IFBIST\_MODE4\_enable.bf | Mode4 programing for RX1 |
| bist/idaSTRX\_RX1\_IFBIST\_MODE5\_enable.bf | Mode5 programing for RX1 |

Table 3 IFBIST sequences for different modes [3]

## IF-BIST and Central Baseband BIST power-on / power -off sequence

In the sequence to turn on the BIST in has to be consider that the dc voltages need to be stablish well before the buffer are enabled. To keep the switches operating in the safe operating point they can only be turned-on when the common mode voltage is stability.

### Turning on/off the BIST-IN amplifier

The Bist-in amplifier can only be turned after the RFBIST amplified is turned on. On the other hand the BIST-IN amplifier and the RFBIST can only be turned off once all the shiches are turned on.

|  |
| --- |
| Assumptions:  * The Rx is already ON.  Power-on Sequence Assume that all the modules are disable   * 1. Turn-on the full baseband BIST   2. Turn-on IF-BIST input buffer **RX: IF\_BIST\_IN\_BUF\_EN**   3. Wait 1us   4. Turn-on IF BIST input switch **RX:IF\_BIST\_A\_SW\_BIST\_TO\_IN**  Power-off sequence Assume that all the modules are enable   1. Turn-off IF BIST input switch **RX:IF\_BIST\_A\_SW\_BIST\_TO\_IN** 2. Wait 1us 3. Turn-on IF-BIST input buffer **RX: IF\_BIST\_IN\_BUF\_EN** 4. Turn-on the baseband BIST |

# RF BIST

This section shows the programing of the BIST logic for measuring the Rx from the LNA input , the mixer input and also to assets the power of the Mixer

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Register name | **Normal operation** | **BIST injection**  LNA-IN | **BIST injection**  Mixer-IN | **BIST Power**  **Measurement**  **LNA IN** | **BIST Power**  **Measurement**  **MIXER IN(note)** |
| rx.lna\_bist.sel\_ip | 0 | 1 | 1 | 1 | 1 |
| rx.lna\_bist.sel\_op | 0 | 0 | 1 | 0 | 1 |
| rx.ldo\_rf\_ctl.ldo\_lna\_en | 1 | 1 | 0 | 1 | 1 |
| rx1.pwr\_ctl.lna\_en | 1 | 1 | 0 | 1 | 1 |
| |  | | --- | | rx.lna\_bist.buf\_en | | rx.lna\_bist.ppd\_en | | rx.lna\_bist.vga\_en | | 0 | 0 | 0 | 1 | 1 |

Table 4 RFBIST programing modes

Note: During calibration of the PPD the circuit needs to be set according to **BIST Power Measurement** mode. This measurement would be used also as estimation for the power when the RF-BIST is measuring the Mixer.

Note: For the assessment of power when the MIXER we can either use the measurement with lna\_bist\_sel\_op or measure the power but with the LDO on.

|  |
| --- |
|  |
| Figure 10 Control for the BIST circuit |

|  |  |
| --- | --- |
| Sequences | Comment |
| idaSTRX\_RX\_RFBIST\_main\_path\_enable\_rfbist\_disable.bf | Normal operation |
| idaSTRX\_RX\_RFBIST\_LNA\_input\_enable.bf | RFBIST in the LNA input |
| idaSTRX\_RX\_RFBIST\_Measure\_LNA\_input\_power.bf | Measured input power when the RFBIST is used at the input of the LNA |
| idaSTRX\_RX\_RFBIST\_MIXER\_input\_enable.bf | RFBIST in the mixer input |
| idaSTRX\_RX\_RFBIST\_Measure\_Mixer\_input\_power.bf | Measured input power when the RFBIST is used at the input of the Mixer |

# ATB

This section describe the ATB

# References

|  |  |
| --- | --- |
| [1] | V. Ilamurugan and J. Osorio, "IF Saturation detector detector," [Online]. Available: https://www.collabnet.nxp.com/sf/go/doc416555?nav=1&pagenum=1&pagesize=15. |
| [2] | F. Harmsze and J. Osorio, "Rx Register Map," [Online]. Available: https://www.collabnet.nxp.com/sf/go/doc445513?nav=1&pagenum=1&pagesize=15. |
| [3] | J. Osorio, "Bitstream for the Rx bist circuit," [Online]. Available: http://strx-c28.ddm.nxp.com:9911/scripts/isynch.dll?panel=DataSheet&url=sync%3a%2f%2f%2fProjects%2fstrx\_es0%2fdata%2fida\_mmw\_rfe\_lib%2fida\_mmw\_rfe\_4tx\_4rx%2fSOFTWARE%2fbitfields\_lib%2fidaStrxAnalog%2fex\_api\_setup%2fRX%2fbist |

# Test Vehicle circuits descriptions

After the TV some the current circuits were modified. The old descriptions are left here for reference.

## IF Saturation detector (TV)

The saturation detector is used in the filter to detect that the level of the signals overpass certain predefined level. There is a complete documentation of this module that can be found in collabned [1]. This section here would focus only in the requirements for the digital circuit. The next figure shows the diagram of the saturation detector.

### Digital functionality

The circuit is made of a digital circuit and analog circuit. The Saturation detector uses a differential latch together with a logarithmic-DAC to achieve a large dynamic range programmability. The saturation detector is reset every 25ns using a pulse that is always small than 2ns. When the signal at the output of the VGA is higher than the voltage output of the log-DAC the flag is stored in a SR and is capture by the digital circuit in the falling edge.

The digital circuit would measure the number of events happening in the analog signal when the signal safety\_monitor\_active\_te is enabled. After an extended period, typically a radar frame, the number of errors are counted and are compared with a programed word of 22bits.

In order to avoid metastability problems the value of the SR latch is sampled in the digital side using a negative-edged flip-flop.

### Saturation DAC range and step

The saturation detector uses la logarithm-DAC to define the value that make triggers it. The DAC is implemented as a logarithm resistor divider which uses as a reference the same LDO that the filter. The saturation detector threshold voltages are defined as:

The dependence of the *vsat* with the voltage of the ldo, *vldo*, is intended as the linearity of the filter depends primarily on the ratio of the output peak signal and the vldo.

|  |
| --- |
| **A picture containing schematic  Description automatically generated** |
| **Figure 11. Saturation detector. A) section of the circuit in the analog side. B) section of the circuit in the digital side. In bold: signals stored in registers, in italic: signals coming from the timing engine.** |

## . LO Level Detector

In order to ensure the mixer it is properly switch it is necessary to verify the level of the LO signal. For that a level detector circuit is used. This circuits is shown in **Figure 12**. The circuit compares the DC output level of the output of the DAC with the rectified version of the 78GHz signal.

### Calibration of the LO level detector

Before every radar cycle the level lo needs to be set such as the reliability of the mixer transistor is maintain. For that the LO level detector is programmed to detect a high level and the Lox2 buffer (TODO: add more reference) is swept until the flag toggles. The LO signal is set one step less.

During acquisition the LO level detector is programmed to detect the minimum acceptable signal in the LO.

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|  |
| **Figure 12: LO Level Detector** |

## Extra description in the saturation detector (Vinoth)

Description of the signals. To do. Is this necessary ?

|  |  |  |
| --- | --- | --- |
| Signal Name | | Description |
| en\_sat\_det\_comp\_pos\_meas | en\_sat\_det\_comp\_neg\_meas |
| 0 | 0 | Normal operating mode. Positive and negative comparators are enabled. |
| 1 | 0 | Enable the positive comparator output and disable the negative comparator output. |
| 0 | 1 | Enable the negative comparator output and disable the positive comparator output. |
| 1 | 1 | Positive and negative comparator outputs are disabled. |

|  |  |  |
| --- | --- | --- |
| Signal Name | | Description |
| en\_sat\_det\_1v5 | en\_zero\_ref\_sat\_det |
| 0 | 0 | Disable the saturation detector. |
| 0 | 1 | Disable the saturation detector. |
| 1 | 0 | Enable the saturation detector. |
| 1 | 1 | Force the differential reference voltage of the positive and negative comparator to 0V. |

# Reviews

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| **t:** | Dear Juan,  My detailed review feedback is provided as red text and comments in the attached document. The majority of the document is very clear but it seems that the document is not fully completed yet. The comments are related to : - missing references - missing description of LO level control loop. - small corrections to text for consistency and clarifications - incomplete power up / power down description - clarification of the error forcing for the saturation detectors - missing timing diagram and some unclarities in description dynamic filter control. - some unclarities in target levels, control signals and timing for LO level control. - some unclarities for calibtation mode of the PPD.  Best Regards, Anton |

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